BRUTE-31P/52P
80C31 & 80C52
(80C52- with Basic Interpreter)
Single Board Controller

Technical Manual
Version 1.2

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Single Board Controller

Technical Manual

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Micromint, Inc
902 Waterway Place
Longwood, FL. 32750

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1.0 BRUTE-31P/52P Overview

The BRUTE-31P/52P is based around Micromint's 80C52 micro-controller. The 80C52 is a CMOS version of Intel's industry standard 8052 micro-controller with a masked internal BASIC interpreter. The built-in BASIC makes DATA acquisition and control accessible to the non-technical user. The experienced programmer can disable BASIC and still reap the benefits of the BRUTE-31P/52P, by ROMing compiled/assembled code written on a PC using your favorite 8031 based language.

BRUTE-31P/52P has a total of 32 TTL level input/output bits. Eight digital inputs have the option of being optically isolated providing non-polarized inputs of up to 18 volts. Eight Digital outputs have the option of open-collector drivers which can sink over 100 mA @ 50 volts (alternate source driver available).

The 12-bit (plus sign) analog to digital converter has either four differential input pairs or eight single ended inputs. The ADC can be hard jumpered for a gain of 1 across all the channels or each channel's gain may be set, to 1, 2, 4, or 8, through software. It can accept voltages in the range of -5 to +5 volts. The ADC's conversion time is 15.68 µS, and conversion start data valid time is 34.5 µS. The 2-channel 12 bit digital to analog converter can have an output range of, 0 to +5 volts, 0 to +10 volts, or -5 to +5 volts.

A real time clock/calendar provides date and time information. An external 3 volt battery will keep the clock (and RAM) alive while the system power is removed. A hardware watchdog timer protects the system from runaway code.

Through paging, one RAM device and one EPROM device share 64k of addressable memory space. The BRUTE-31P/52P has 32k of Data space and 56k of Program space available. When configured as a BRUTE-52P the 32k of data space starts at address location 0000H and the 56k of program space starts at 8000H.

The BRUTE-31P/52P operates on +12, -12, and +5 volts. It has one and a half serial ports capable of communicating RS232 or RS485. Brute-52P shares the same platform but uses an 80C52 BASIC chip as its processor. Together they provide an unbeatable combination of high-performance I/O with the programming ease of a high speed, ROM-resident BASIC.

2.0 80C31 Vs. 80C52

The 80C51 family of control-oriented CPUs was first introduced by Intel in the early 1980s. Since that time, many companies including AMD, Fujitsu, GE/Intersil, Philips, Siemans, and Dallas have second-sourced one or more devices in this family. This kind of competition shows the 80C51 family as a dominating faction in the embedded-controller industry. Two popular versions in this family are the 80C31 and 80C52. The internal differences are as follows:

DIFFERENCES	80C31	80C52
RAM		
Internal	128 x 8 bits	256 x 8 bits
External	64k x 8 bits	64k x 8 bits
ROM		
Internal	none	8k x 8 bits
External	64k x 8 bits	56k x 8 bits (64k x 8 bits when not using t internal ROM)
Timer/Counter	2 x 16 bits	3 x 16 bits
Interrupts		
Internal	3	4
External	2	2

They also have many features in common, as seen below:

COMPARABLE	80C31	80C52
PORTS	4 x 8 bits	4 x 8 bits
Execution Time @ 12 MHz Clock INSRUCTION		
1 byte	1 Microsecond	1 Microsecond
2 bytes	2 Microsecond	2 Microsecond
3 bytes	4 Microsecond	4 Microsecond

The instruction set of the 80C51 family of microcontrollers is similar to the 8048 family, with the addition of:

Non paged Jumps
Direct Addressing
Four 8 bit Register Banks
Stack Depth Up to 128 Bytes
Multiply, Divide, Subtract, and Compare

3.0 External Addressing Space

The BRUTE-31P/52P can directly address 96k of external memory. That is, 32k of DATA memory, 56k of PROGRAM memory, and 8k of I/O devices. The *RD and *WR lines control the DATA memory and the *PSEN line controls the PROGRAM memory. Overlapped space occurs when the *RD and *PSEN lines are combined. A combined DATA/PROGRAM space is useful when CODE must be executed out of RAM for various reasons.

When using the BRUTE-52P with BASIC, RAM must be at 0000H. When using the BRUTE-52P with out BASIC, compiled/assembled code (your EPROM) must start executing at 0000H.

3.1 Memory Size and Location Selection

Two memory sockets are provided on the BRUTE-31P/52P board (U10 & U11). The DATA space (U10) is always configured for 32k of addressable space. The PROGRAM space has two jumpers associated with it (JP5 and JP7). JP5 selects the size of the PROM for U11. U11 can have an 8k EPROM (Figure 1A), 16k EPROM (Figure 1B), 32k EPROM (Figure 1C), or 64k EPROM (Figure 1D) EPROM. It can also have a 8k EEPROM (Figure 1E) or 32k EEPROM (Figure 1F). JP7 selects the location of the PROGRAM memory, either 0000H (Figure 2A) or 8000H (Figure 2B).

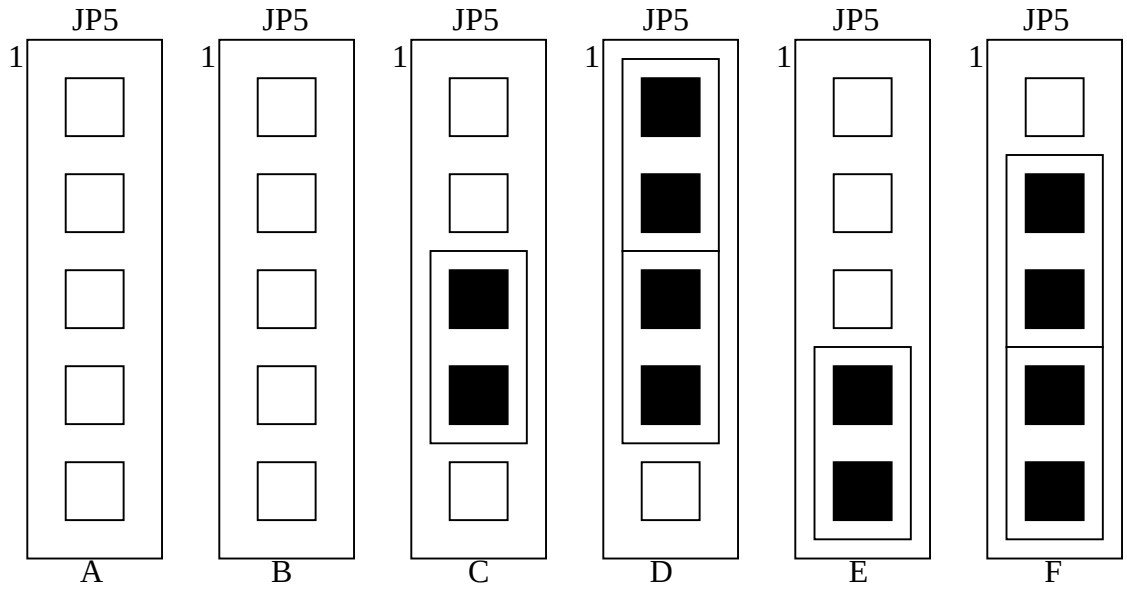


Figure 1: JP5 PROM **m**emory size selection for U11.

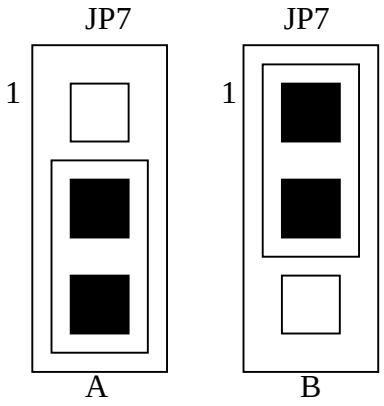


Figure 2: JP7 PROGRAM memory location.

3.2 Memory Space Type

By ORing the *RD and *PSEN lines, a combined DATA/PROGRAM space can be created for U10. This allows the ease of development by using a BOOT ROM in U11 to develop and run your program in RAM. JP4 allows you to make U10 DATA/PROGRAM (Figure 3A) or just DATA space only (Figure 3B).

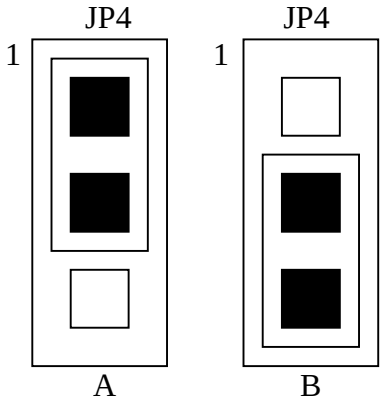


Figure 3: JP4 memory space type for U10

3.3 RAM Battery Backup Selection

The RAM on the BRUTE-31/52P is capable of storing DATA while the system power is OFF. DATA retention time depends on battery and RAM selection. Use RAMs with a typical standby current of 1µA. This requires about 10mAHr/year of battery current. (The OKI clock/calendar on the BRUTE 31P/52P requires about 100mAHr/year.

Precautions must be taken, when using the BASIC interpreter and battery backed RAM. **A reset will normally clear all RAM.** Please refer to the PROG3 - PROG6 commands for protecting RAM, located in the BASIC-52 programming manual.

VCC and *CE for the RAM is controlled by the MAX691. This device monitors +5 volts and switches in the battery backup battery when +5 volts is not within tolerance. Additionally, if out of tolerance, it prevents the *CE from enabling the RAM which could result in an unwanted write (usually during power-up and

power-down). JP6 gives the user the option to battery backup the RAM (Figure 4A) or not to battery backup the RAM (Figure 4B).

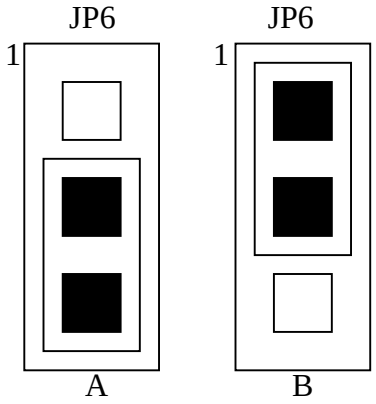


Figure 4 : JP6 battery backing the RAM

3.4 External Code Space

The 80C31 microcontroller requires *EA to be pulled down to a logic low level. This instructs the processor to start executing machine language code at address 0000H (PROGRAM space). The 80C52's, internal 8k ROM is masked with a BASIC interpreter and will run internal code (BASIC interpreter) if *EA is pulled up to a logic high. Pulling *EA low on an 80C52 will disable the BASIC interpreter and execute code starting at 0000H (similar to an 80C32). Installing a jumper on JP1of the BRUTE-31P/52P will pull the *EA pin low.

4.0 Resetting the BRUTE-31P/52P

The reset function of the BRUTE-31P/52P is handled by U6 (MAX691). The MAX691 holds the *RESET line low until the supply is within tolerance for 50 milliseconds. This exceeds the processor's minimum necessary startup time of 24 cycles.

4.1 Reset Source

The *PFO (power fail output) is wire-OR'd to the *RESET line, and thus can cause a system reset. This signal goes low whenever the PFI (Power Fail Input) falls below 1.3V. The PFI has two sources on the BRUTE-31P/52P; *IOKI (clock calendar interrupt) and *INT0 (P3.2). The two reset sources are selected through JP3. Figure 5A demonstrates the system being reset by *INT0 and Figure 5B demonstrates the system being reset by *IOKI.

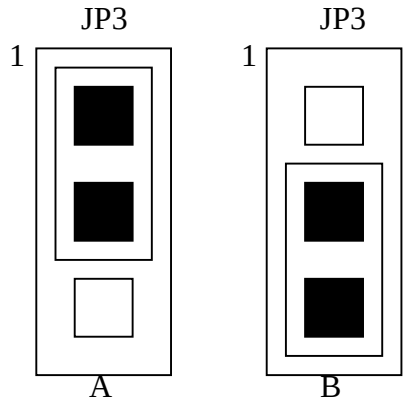


Figure 5: JP3 System reset sources.

4.2 Watchdog Source

The MAX691 also has a hardware watchdog function. If the jumper on JP2 is not installed, the watchdog is disabled and produces no *RESET pulse. However, if the WDI (watchdog input) is pulled up or down, an internal 1.6 second timer starts. Upon time-out, a 50 millisecond *RESET pulse is produced. To prevent the watchdog timer from resetting the system, the WDI must change states to restart the 1.6 second timer. This can come from one of two sources. The *IOKI (OKI clock/calendar interrupt, Figure 6A) can be programmed to produce a 1 second interrupt or T1 signal (P3.5, Figure 6B) can be directly toggled from the processor. The user must maintain a constant restarting of the WDI timer to insure the program will not be inadvertently RESET. If a program crash should occur, the WDI timer will not be restarted and a *RESET will initiate a "warm start".

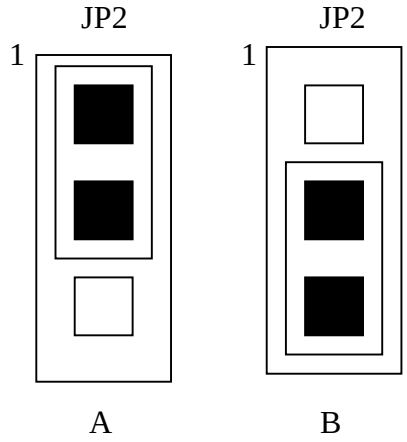


Figure 6: JP2 Watchdog input sources.

5.0 Serial Communications

The BRUTE-31P/52P has one serial communications port. It can be configured to communicate using either RS-232 (U21) or RS-485 (U20). If the serial port is configured for RS-232 then U20 should be removed from the board to eliminate the possibility of any noise interfering with serial communications and the receive line should be jumpered for RS-232 communications (Figure 7A). If configured for RS-485 then

U21 should be removed for the same reason and the receive line should be jumpered for RS-485 communications (Figure 7B).

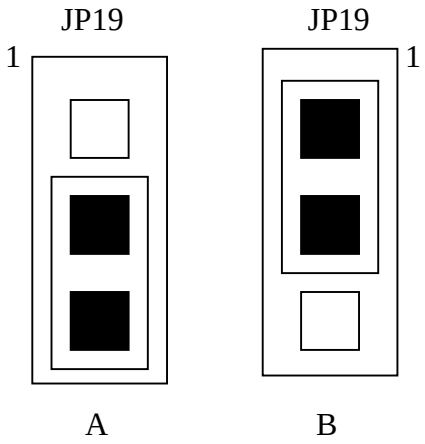


Figure 7: JP19 receive communication selection.

RS-232 is a full-duplex transmission path using three wires. Use RS232 with a terminal or computer. RS-485 is a half-duplex transmission path using two wires. Use RS-485 for twisted pair and multi-drop installations. RS-485 requires software to control the direction of transmissions to eliminate multiple driving sources.

5.1 RS-232 Communication

The user's standard communications interface is through the RS-232 Console port. This port can be used to send and receive programs and data to and from the BRUTE 31P/52P processor. The BRUTE 52P will auto-baud detect (a space character) from 300-9600 baud or can be programmed to auto-start a 'saved' BASIC program at a particular baud rate.

An RS-232 connection is made to a terminal device using a simple 'straight through' cable. A ribbon cable with a DB-25S at one end and a 2X8 square-pin connector at the other end is easily made using locally available parts, or purchased directly from Micromint.

The TTL serial I/O lines are converted from/to RS-232 by U21. This device has internal charge pumps and an inverter to create the necessary plus and minus voltages for RS-232. The serial port does not use hardware handshaking, so pull-up resistors are provided on RS-232 handshaking lines which may be required by some connecting equipment. Figure 8 is the pin out of the Console RS-232 port.

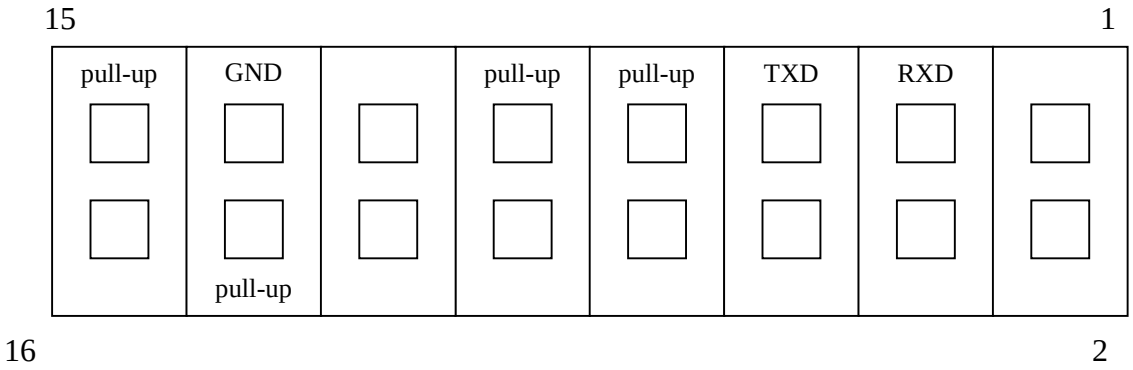


Figure 8: J5A Console RS-232 Port

The BRUTE-52P also has a serial printer port on PORT1.7 of the processor I/O, that is available using the PRINT# or PH0# BASIC command. To print, P1.7 (Auxiliary RS-232 Port) must be connected to the RS-232 chip (U21). Since the BRUTE 31P/52P is also designed for a Dallas 80C320 processor JP20 must be used to connect PORT1.7 to U21 (Figure 9A). If a program is written to print out PORT1.3 then JP20 must be configured like Figure 9B.

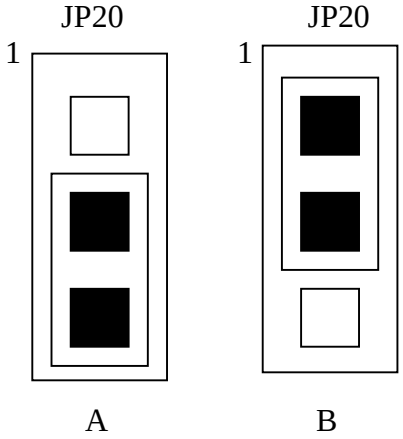


Figure 9: JP20 Auxiliary RS-232 Port selection jumper.

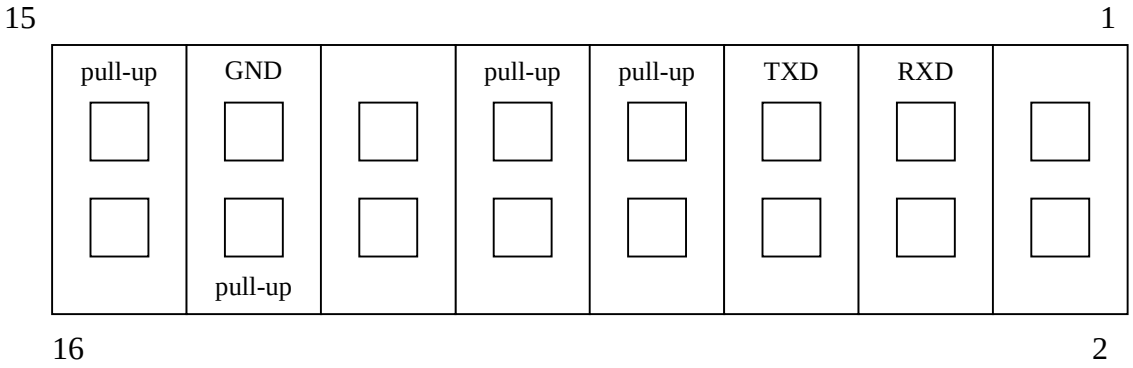


Figure 10: J5B Auxiliary RS-232 port.

5.2 RS-485 Communications

Half-duplex RS-485 communication is a bit trickier to implement. The activity on this differential pair must be closely choreographed since it should only be initialized from one source at a time. The RS-485 driver/receiver allows up to 32 devices to share one twisted pair of wires. Adding additional devices requires an RS-485 expansion booster. The screw terminals marked T1 (Figure 11) on the circuit board are the connections for RS-485.

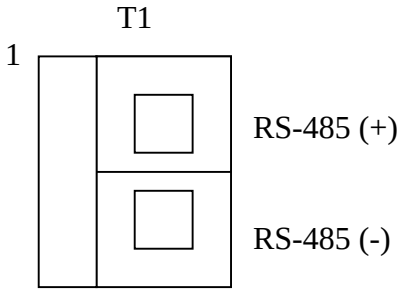


Figure 11: T1 RS-485 Connection.

To eliminate the possibility of more than one device talking on the communication line, a simple master/slave arrangement is suggested. Use your PC as the master and the BRUTE-31P/52P as a slave. The PC takes over the line and asks a question and releases the line. Then the BRUTE-31P/52P seizes the line, answers the question, and releases the line. With this method the BRUTE-31P/52P remains in receive mode until it receives a request for information. Multiple BRUTE-31P/52Ps can be added to the communication bus if each board is assigned a special address (in your software) and does not respond to a request unless the request contains the matching address information.

RS-485 requires termination resistors on the network for it to operate properly. On any RS-485 network the first and last device on the network need to have terminating resistors and a 100 ohm resistor between the two lines (Figure 12A). All devices in the middle of the network also need a 100 ohm resistor between the two lines (Figure 12B).

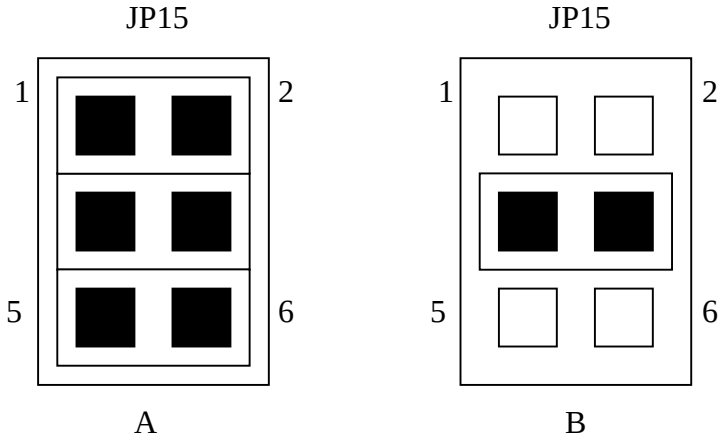


Figure 12: JP15 RS-485 Termination Resistors.

The transmit line on the RS-485 driver is turned on by setting bit P3.4 (T0 in the 80C52). The RS-485 receiver is turned on by clearing bit 3.4 in the micro-controller. When using the 80C52's BASIC interpreter this bit is not accessible through BASIC. It can only be accessed through an assembly language CALL statement. A two statement machine language routine is all that is necessary.

To enable transmit driver:

```
0D2H 0B4H        SETB T0
22H              RET
```

To enable receiver:

```
0C2H 0B4H        CLR T0
22H              RET
```

The code for these two routines (6 bytes) can be hard coded into your EPROM or poked into RAM using DATA statements from a BASIC program.

6.0 Digital Inputs/Outputs

The BRUTE-31P/52P has 32 bits of digital I/O. Eight bits are directly accessible through the processor's PORT1 (connector J8). The BRUTE-31P/52P as an on-board 82C55 programmable peripheral interface chip that provides three 8-bit parallel I/O ports (connector J3).

6.1 Non-TTL Inputs

BRUTE-31P/52P has the option of having eight optically isolated non-polarized inputs. Each input pair is totally isolated from the system and one another. The inputs are non-polarized so they aren't sensitive to the polarity of the signal or the connection direction. The isolators are connected to port A of the BRUTE-31P/52P's PPI (82C55). Pull-ups on port A inputs are read as "logic 1" when less than ±1.3 volts is applied to any non-TTL input bit on J2 (Figure 13). "Logic 0" is read on any port A bit that has greater than ±2.6 volts applied to it's non-TTL input bit on J2, pulling its port A input bit to ground. **Note that this is 'Inverted LOGIC'. If using port A as non-TTL inputs remember not to connect anything to the corresponding bit on J3. The mode of the 82C55 must be programmed by the user (section 6.3).**

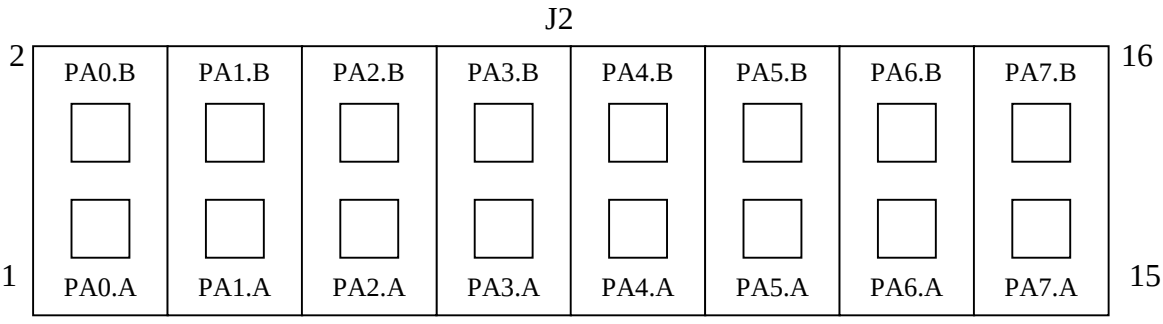


Figure 13: J2 Opto-Isolated Inputs for Port A.

6.2 Non-TTL Outputs

BRUTE-31P/52P has the option of having eight open-collector high-voltage/ high-current outputs. Port B of U15 (82C55) controls the high-voltage/high-current outputs on J4 (Figure 14). Four of the pins on J4 are designated as External Voltage Inputs and four as External Voltage Ground Inputs. This External Voltage

must be provided by the user and will be used for all eight open-collector outputs. Since the outputs are open-collector, they must have a pull-up (or load) added between each output and the External Voltage. The outputs will be pulled to ground (1.6V Max) when a "logic 1" is written to the appropriate bit of the PPI's Port B register. **The mode register must be programmed by the user to set up Port B as output (Section 6.3). If using port B as non-TTL outputs please remember not to connect anything to the corresponding bit on J3.** A "logic 0" will allow the drivers to return to their high-state.

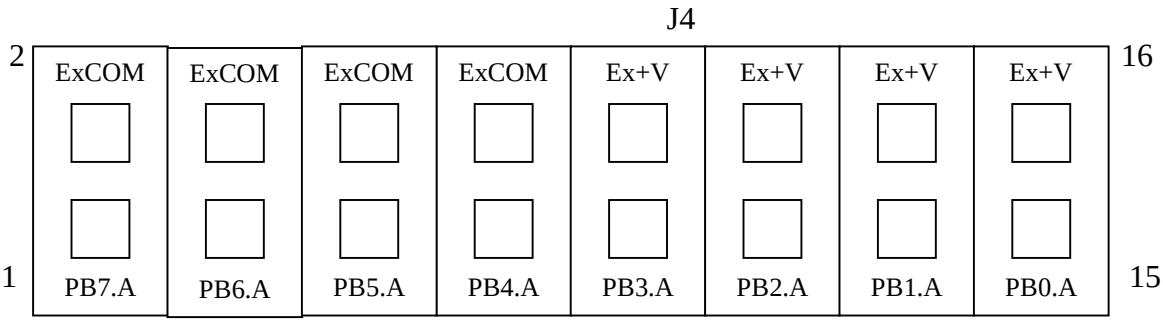


Figure 14: J4 Open-collector Outputs for Port B.

If an open-collector current source is needed, the user can substitute a UDN2981A for U16 (ULN2803A). With this arrangement the outputs should have a load added between each output of the External Voltage Common (pull down).

Jumpers JP12 - JP14 (Figure 15) select the type of output driver used. These jumpers determine how the External Voltage and Common are connected to the system.

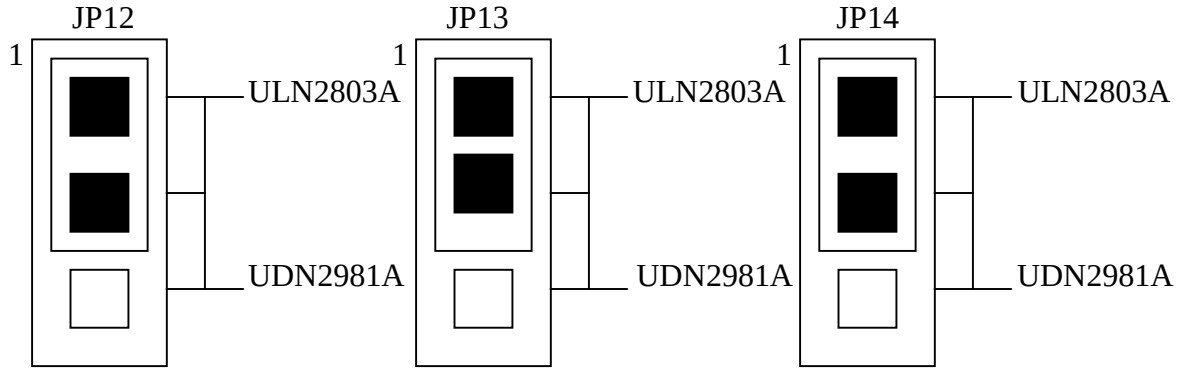


Figure 15: JP12-JP14 Device Selection for Non-TTL Ouputs.

6.3 82C55 Programmable Peripheral Interface (PPI)

The 82C55 programmable peripheral interface (PPI) is an efficient and cost-effective way to add TTL (logic level) I/O to any micro-controller system. One PPI adds 24 bits of I/O to the BRUTE-31P/52P system. The 24 bits are grouped into three 8-bit input or output ports. Port A and Port B can be independently programmed as 8-bits of inputs or 8-bits of outputs. Port C is divided into two 4-bit nibbles (an upper and lower nibble). These nibbles can be programmed independently as 4-bits of inputs or 4-bits of outputs.

The ports are memory mapped into the DATA space of the BRUTE-31P/52P. The PPI has a base address of 0E000H. Port A is available through address 0E000H. Port B is available through address 0E001H. Port

C is available through address 0E002H. The MODE port is a write-only port used to set the PPI for the appropriate configuration. The MODE Port is available through address 0E003H. Figure 16 lists all of the available modes and the corresponding values.

82C55 Configuration				
Port A	Port B	Port C Upper Nibble	Port C Lower Nibble	Mode Value
INPUTS	INPUTS	INPUTS	INPUTS	09BH
INPUTS	INPUTS	INPUTS	OUTPUTS	09AH
INPUTS	OUTPUTS	INPUTS	INPUTS	099H
INPUTS	OUTPUTS	INPUTS	OUTPUTS	098H
INPUTS	INPUTS	OUTPUTS	INPUTS	093H
INPUTS	INPUTS	OUTPUTS	OUTPUTS	092H
INPUTS	OUTPUTS	OUTPUTS	INPUTS	091H
INPUTS	OUTPUTS	OUTPUTS	OUTPUTS	090H
OUTPUTS	INPUTS	INPUTS	INPUTS	08BH
OUTPUTS	INPUTS	INPUTS	OUTPUTS	08AH
OUTPUTS	OUTPUTS	INPUTS	INPUTS	089H
OUTPUTS	OUTPUTS	INPUTS	OUTPUTS	088H
OUTPUTS	INPUTS	OUTPUTS	INPUTS	083h
OUTPUTS	INPUTS	OUTPUTS	OUTPUTS	082h
OUTPUTS	OUTPUTS	OUTPUTS	INPUTS	081H
OUTPUTS	OUTPUTS	OUTPUTS	OUTPUTS	080H

Figure 16: 82C55 MODE Configuration Table

The 82C55's reset pin has the option of being reset when the whole system does (Figure 17A) or only reset upon power up (Figure 17B). Upon power-up or manual reset, the PPI is configured with all three ports (A, B, &C) as inputs. Once reconfigured, if necessary for your application, care must be taken not to change the mode. The values at each port will be lost when the mode is changed.

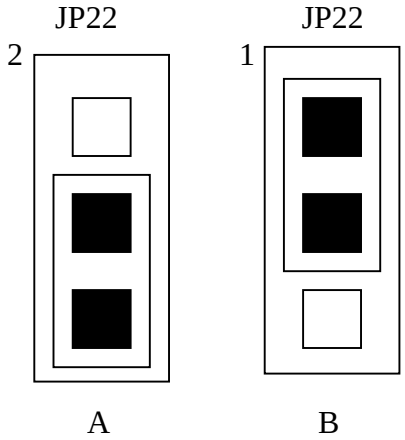


Figure 17: JP22 82C55 Reset Options.

The 82C55 ports are brought out to connector J3. J3 is populated with a 2X25 square pin header. **NOTE: If using port A as non-TTL inputs remember not to connect anything to the corresponding bit on J3. If using port B as non-TTL outputs please remember not to connect anything to the corresponding bit**

on J3. The following program will allow easy configuration of the I/O ports and testing of the TTL I/O pins on J3.

6.4 Sample BASIC-52 Program for the PPI

```
 10 STRING 91,9
 20 $(0)="OUTPUT" : $(1)="INPUT" : $(2)="WRITE" : $(3)="READ"
 30 P=0E000H
 40 A=1 : B=1 : C=1 : M=9BH : XBY(P+3)=M
 50 PRINT
 60 PRINT "8255 Parallel Port test on U19 @ 0E000H using JP17"
 70 PRINT  :  PRINT "Hit MENU Selection #" :  PRINT
 80 PRINT "  remember -- changing the MODE of A, B, or C will affect"
 90 PRINT "       DATA previously written to any port)"
100 PRINT
110 PRINT "1 - Set Port A from ",$(A)," to ",$(ABS(A-1))
120 PRINT "2 - ",$(A+2)," PORT A"
130 PRINT "3 - Set Port B from ",$(B)," to ",$(ABS(B-1))
140 PRINT "4 - ",$(B+2)," PORT B"
150 PRINT "5 - Set Port C from ",$(C)," to ",$(ABS(C-1))
160 PRINT "6 - ",$(C+2)," PORT C"
170 PRINT "7 - END"
180 G=GET
190 G=GET
200 IF G=0 THEN 190
210 G=G-30H
220 IF ((G<1).OR.(G>7)) THEN 190
230 IF G=7 THEN  END
240 ON G-1 GOSUB 260,530,350,590,440,650
250 GOTO 50
260 IF A=1 THEN 310
270 A=1
280 M=M.OR.10H
290 GOSUB 710
300 RETURN
310 A=0
320 M=M.AND.8FH
330 GOSUB 710
340 RETURN
350 IF B=1 THEN 400
360 B=1
370 M=M.OR.02H
380 GOSUB 710
390 RETURN
400 B=0
410 M=M.AND.0FDH
420 GOSUB 710
430 RETURN
440 IF C=1 THEN 490
450 C=1
460 M=M.OR.09H
470 GOSUB 710
480 RETURN
490 C=0
500 M=M.AND.0F6H
510 GOSUB 710
520 RETURN
530 IF A=1 THEN 570
```

```
540 INPUT "Enter Value"V
550 XBY(P)=V
560 RETURN
570 PH0. XBY(P)
580 RETURN
590 IF B=1 THEN 630
600 INPUT "Enter Value"V
610 XBY(P+1)=V
620 RETURN
630 PH0. XBY(P+1)
640 RETURN
650 IF C=1 THEN 690
660 INPUT "Enter Value"V
670 XBY(P+2)=V
680 RETURN
690 PH0. XBY(P+2)
700 RETURN
710 XBY(P+3)=M
720 RETURN
```

7.0 Analog to Digital Converter

The ADC section of the BRUTE-31P/52P consists of three parts, a multiplexer (U13), a programmable gain amplifier (U19), and the actual ADC (U22). Accessing the analog-to-digital converter is simple and consists of two write and three read statements.

7.1 Analog Input Connector - J1

The analog input signals are brought onto the board through connector J1. Figure 18A shows how the connector is laid out for eight single ended channels of ADC. Figure 18B shows how the connector is laid out for four differential channels of ADC.

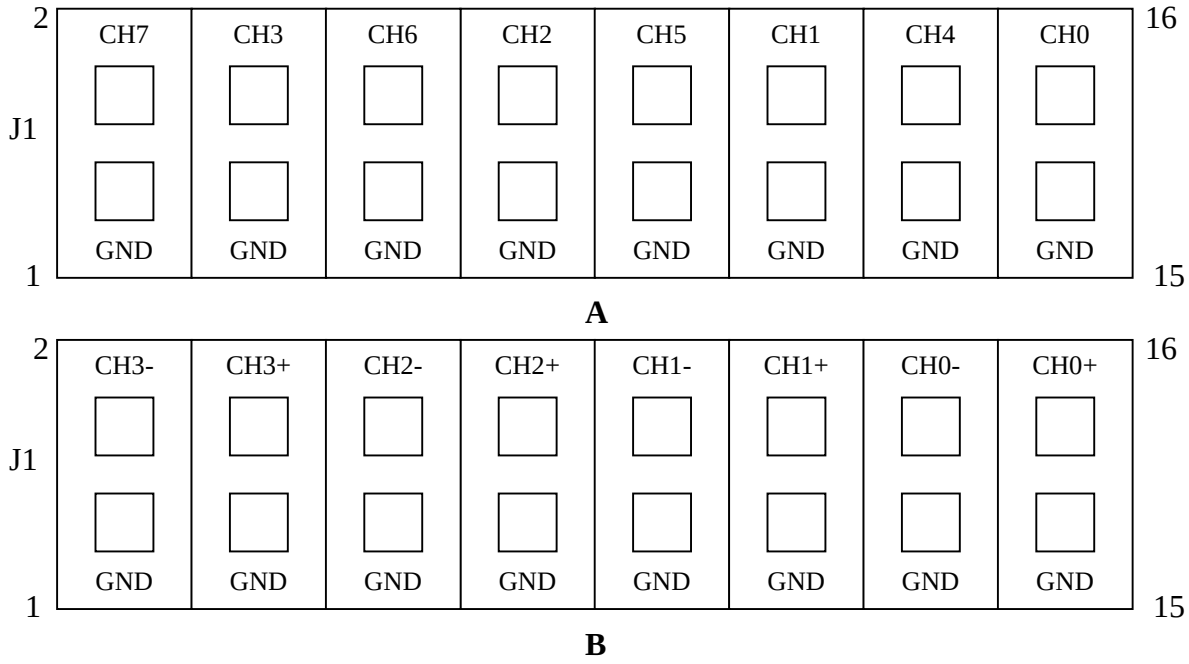


Figure 18: J1 Analog Input Connector.

7.2 The ADC Conversion Process

Each time a conversion starts, the ADC automatically goes through an auto-zero cycle to minimize zero errors. The ADC can also be put into an auto-calibrate cycle by pulling its *CAL pin low. The auto-calibrate cycle will correct zero, full-scale, and linearity errors. To start the auto-calibrate cycle a dummy value is written to the address 0E0C0H. For example:

XBY(0E0C0H) = 0 (inBASIC-52)

To read an analog input the channel number and gain must be sent to address 0E080H. The control word which defines the channel and gain is configured as in Figure 19.

ADC Control Word							Address = 0E080H
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

		Gain
0	0	1
0	1	2
1	0	4
1	1	8

			Channel
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Figure 19: ADC Control Word Table.

Note that bits 3, 4, and 5 are not used. From Figure 19 we can see that if we want to read channel 0 with a gain of 1 the control word would be 00H. If we wish to read channel 6 with a gain of 4, the control word would be 86H.

The End of Conversion (EOC) status bit is used to detect when a conversion is complete. The EOC status bit is obtained by reading the address 0E0A0H. **The EOC bit will be low (logic 0) during a conversion or when the analog-to-digital converter is in it's calibration cycle. The bit will be high (logical 1) when a conversion is completed.**

EOC Status Word							Address = 0E0A0H
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	X	X	EOC

Figure 20: EOC Status Word

To determine the status of the conversion, a dummy value is first written to the EOC bit. The conversion is then started and the EOC bit is read. Once the EOC bit goes high the conversion is completed.

After it has been determined that the conversion is complete, the data may be read. This is accomplished by doing two read of the analog-to-digital converter at address 0E080H. The first read produces four most significant bits and the sign bit (Figure 21A). The second read produces the eight least significant bits (Figure 21B).

MSB & Sign							Address = 0E080H
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sign	Sign	Sign	Sign	Bit 11	Bit 10	Bit 9	Bit 8

Figure 21A: Most Significant Bits and Sign.

LSB							Address = 0E080H
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Figure 21B: Least Significant Byte.

Reading the ADC can be broken down into four steps.

1 - Reset the EOC status by writing a dummy value to it.
2 - Send a control word containing the gain and channel number to start the conversion.
3 - Wait for EOC.
4 - Read the data from the ADC.

7.3 Sample BASIC-52 Program for the ADC

```
 10 REM BASIC-52 - BRUTE 52P Sample Program
 20 REM **** Address Initialization ****
 30 ADCB = 0E080H
 40 ADCC = 0E0C0H
 50 ADCE = 0E0A0H
 60 REM **** Calibrate the ADC ****
 70 XBY(ADCE)=0
 80 XBY(ADCC)=0
 90 IF ((XBY(ADCE).AND.1)=0) THEN 90
100 REM ** Choose a channel, set the gain, and read the channel **
110 INPUT "Select a channel(0-7)",CHNL
120 INPUT "Select a gain (1,2,4,8)",GN
130 IF GN=1 THEN GN=0H
140 IF GN=2 THEN GN=40H
150 IF GN=4 THEN GN=80H
160 IF GN=8 THEN GN=0C0H
170 XBY(ADCE)=0
180 XBY(ADCB) = (GN+CHNL)
190 IF ((XBY(ADCE).AND.1)=0) THEN 190
200 ADCH = XBY(ADCB)
201 ADCH=ADCH.AND.1FH
210 ADCL = XBY(ADCB)
220 IF (ADCH<16) THEN ADC=((256*(ADCH.AND.15)+ADCL)/4096)*5
230 IF (ADCH>15) THEN ADC=-(((1FFFH.XOR.(256*ADCH+ADCL))+1)/4096)*5
240 ?"Channel ",CHNL, " reads ",ADC," volts"
250 GOTO 110
```

7.4 Differential versus Single-ended Inputs

The previous discussion and sample code have dealt with using the BRUTE-31P/52P in single-ended mode (Figure 22A). Using the board in differential mode is very similar. In single-ended mode the signal being measured is referenced to the ground of the BRUTE-31P/52P. In differential mode the signal is not referenced to ground (Figure 22B).

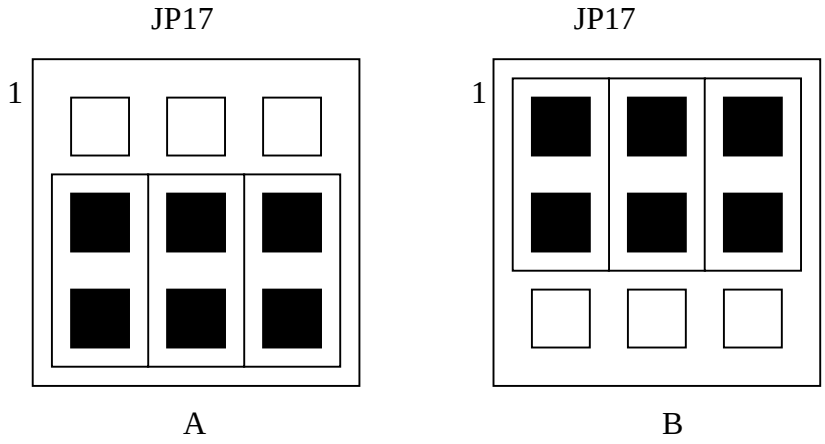


Figure 22: JP17 ADC Mode Selection.

8.0 Digital to Analog Converter

The digital-to-analog converter (DAC) has the capability to output -5V to +5V, 0V to +5V, or 0V to +10V.

8.1 Analog Output Modes

The analog output signals are brought out through 2 screw terminals (T2 and T4). Channel 0 is brought out through T2, and Channel 1 is brought out through T4 (Figure 23).

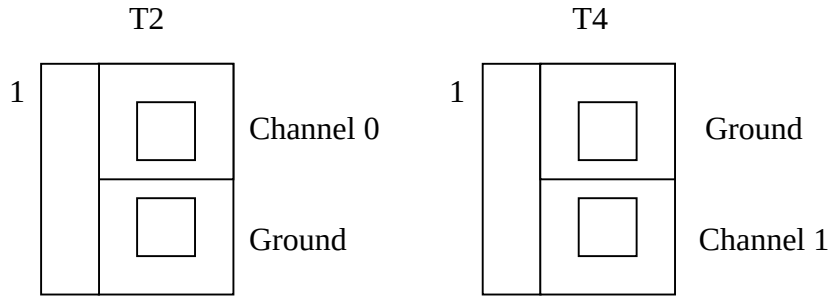


Figure 23: Analog Output Screw Terminals

The output of each channel can be set to one of three ranges: 0V to +5V, 0V to +10V, or -5V to +5V. Selection is accomplished through jumpers JP9 for channel 0 (Figure 24) and JP10 for channel 1 (Figure 24). **Please refer to the silk screen for the location and orientation of these jumpers.**

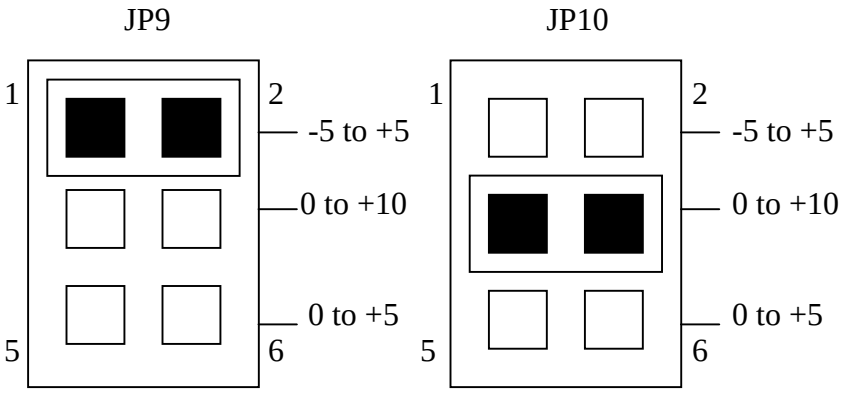


Figure 24: Analog Output Range Selection Jumpers

The 0 to +10V output mode is a special case. The maximum output of a channel configured in this mode is approximately 80% of the +12V supply. For example, if your +12V supply is actually supplying 11.8 volts then the maximum output of the DAC will be approximately 9.44 volts. This anomaly does not change the relationship between data input to the DAC and the output. Sending 0 to the channel will still result in a 0V output and sending 2048 (800H) will still result in a +5V output. The only difference that will be noted is the maximum voltage which can be output.

8.2 The DAC Conversion Process

Control of the DAC is accomplished by writing a value to the input latches and transferring the data to the output. Each channel has two input latches associated with it, the 4-bit most significant and the 8-bit least significant. Either of these latches may be written to first. Writing to the latches is quite simple. For example, if channel 1 is configured for the -5V to +5V output range and we wish to have a 4V output then the following must be done.

10V (output range) ÷ 4096 = 0.00244V (resolution)

Since the range is -5V to +5V then 0 = 2048 = 800H. So if the value to be output is greater than or equal to zero then we must add 2048 (800H) to it.

4V ÷ 0.00244V = 1639 = 667H
1639 + 2048 = 3687 = value sent to the DAC
OR
667H + 800H = E67H = value sent to the DAC

MS 4-Bits	LS 8-Bits
E	67

With this information we are now ready to write the data to the DAC. The base address of the DAC is 0E060H (Figure 25). Using our example to set channel 1 to 4V, write 0EH to 0E063H and 67H to 0E062H. Then write a dummy value to 0E050H to transfer the data to the output.

	MSB Address	LSB Address
Channel 0	0E061H	0E060H
Channel 1	0E063H	0E062H

Figure 25: DAC channels addresses

It is important to note that when a transfer has begun, the data for both channels is transferred from the input latches to the outputs at the same time. Because of this you can load the input latches for both channels and then do a transfer. This will update both outputs simultaneously.

8.3 Sample BASIC-52 Program for the DAC

```
 10 REM Brute 52P DAC sample
 20 PRINT
 30 REM **** addresses
 40 base = 0E000h
 50 T01 = 50H
 60 REM **** Select a channnel
 70 PRINT
 80 INPUT "Select a channel (0,1) ",CH
 90 IF CH=0 THEN CH=60H
100 IF CH=1 THEN CH=62H
110 PRINT
120 REM **** Select an output range
130 ?"What output range is selected by JP9 and JP10?"
140 ?" 1   -   -5 to +5V"
150 ?" 2   -    0 to +5V"
160 ?" 3   -    0 to 10V"
170 INPUT "Enter your choice (1,2,3) ",RG
180 PRINT
190 REM **** Select a voltage to output
200 INPUT "Enter the voltage you wish to output. ",V
210 PRINT
220 REM **** Convert and output
230 ?"Converting the data and setting the output ..."
240 IF RG=2 THEN  GOTO 370
250 IF RG=3 THEN  GOTO 440
260 IF (V<0) THEN  GOTO 290
270 V = (INT(V/0.0024415)) + 2048
280 GOTO 310
290 V=(5+V)
300 V=(V/0.00244)
310 MSB=(V.AND.0F00H)/0FFH
320 LSB=V.AND.0FFH
330 XBY(BASE+CH)=LSB
340 XBY(BASE+CH+1)=MSB
350 GOSUB 510
360 GOTO 70
370 V=(INT(V/0.0012207))
380 MSB=(V.AND.0F00H)/0FFH
390 LSB=V.AND.0FFH
400 XBY(BASE+CH)=LSB
410 XBY(BASE+CH+1)=MSB
420 GOSUB 510
430 GOTO 70
440 V=INT(V/0.002442)
```

```
450 MSB=(V.AND.0F00H)/0FFH
460 LSB=V.AND.0FFH
470 XBY(BASE+CH)=LSB
480 XBY(BASE+CH+1)=MSB
490 GOSUB 510
500 GOTO 70
510 XBY(BASE+T01)=0
520 RETURN
```

9.0 Real Time Clock /Calendar

Data collection and control applications are usually time dependent. The addition of a hardware clock/calendar can relieve the micro-controller from any time keeping operations. OKI's M6242B CMOS clock/calendar (U14) has both a clock/calendar and selectable interrupt outputs. Thirteen registers hold time and date information and three registers are used for control purposes. These registers are addressed by the latched addresses A0-A3. Each register is a nibble wide. The lower 4 bits of the data value are significant. Each value is between 0 and 15, most are from 0 to 9 (a decimal digit). Please refer to Figure 25 for the clock/calendar register addresses and descriptions.

M6242B Real Time Clock/Calendar Register Table								
Register		DATA				DATA		
Number	Name	D3	D2	D1	D0	Limit	Description	Address
0	S1	s8	s4	s2	s1	0-9	1-second digit	0E020H
1	S10	**	S40	s20	s10	0-5	10-second digit	0E021H
2	M1	Mi8	Mi4	mi2	mi1	0-9	1-Minute Register	0E022H
3	MI10	**	Mi40	mi20	mi10	0-5	10-Minute Register	0E023H
4	H1	h8	h4	h2	h1	0-9	1-Hour Register	0E024H
5	H10	**	PM/AM	h20	h10	0-2/0-1	PM/AM 10-hour digit	0E025H
6	D1	d8	d4	d2	d1	0-9	1-Day Register	0E026H
7	D10	**	**	d20	d10	0-3	10-Day Register	0E027H
8	MO1	Mo8	Mo4	mo2	mo1	0-9	1-Month Register	0E028H
9	MO10	**	**	**	mo10	0-1	10-Month Register	0E029H
10	Y1	y8	y4	y2	y1	0-9	1-Year Register	0E02AH
11	Y10	y80	Y40	y20	y10	0-9	10-Year Register	0E02BH
12	W	**	w4	w2	w1	0-6	Week Register	0E02CH
13	CD	30 sec	IRQ	BUSY	HOLD		Control Register D	0E02DH
14	CE	t1	t2	IRT/ST	MASK		Control Register E	0E02EH
15	CF	TEST	24/12	STOP	REST		Control Register F	0E02FH

Figure 26: Optional Real Time Clock/Calendar Register Table.

There are two procedures for writing and reading the clock/calendar information. Both procedures are similar with the exception of the hold and busy bits.

The first method involves setting the HOLD-bit to a '1' and checking the busy bit. If the busy bit is '1' then reset the HOLD-bit to '0' and start the sequence again. If the BUSY-bit is '0' then write or read any registers as needed. The HOLD-bit should not exceed 1 second or it will be lost.

The second method disregards the HOLD and BUSY bits. The appropriate register is read from or written to and to ensure a proper read or write, a verify read must be performed. If a discrepancy is found, a correction is made and reverified.

9.1 Register Functions of the M6242B

S1, S10, MI1, MI10, H1, H10, D1, D10, MO1, MO10, Y1, Y10, AND W

These registers are abbreviations for SECOND1, SECOND10, MINUTE1, MINUTE10, HOUR1, HOUR10, DAY1, DAY10, MONTH1, MONTH10, YEAR1, YEAR10, and WEEK. The values are BCD notation (e.g. s8, s4, s2, s1 = 1001H or nine). Data values written outside the limit will cause erroneous read back results. The PM/AM bit must be set if using 12-hour mode. Leap years are recognized and an illegal date will be corrected to the next correct date on the next day rollover. The day of the week register is defined in Figure 27.

Day of the Week Register			
w4	**w2**	**W1**	**Weekday**
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

Figure 27: M6242B Day of the Week Register

9.2 Control D Register

HOLD (D0) Setting this bit to a '1' inhibits the 1-Hz S1 counter. A carry is held from the S1 counter until HOLD=0 providing HOLD isn't greater than 1 second.

BUSY (D1) Status of interface condition. '1' indicates BUSY.

IRQ (D2) Status of the STD.P (OUT) output. '1' indicates an interrupt has occurred. Resetting this to a '0' will clear the interrupt. The IRQ FLAG must be a '1' when writing to the HOLD or 30 SEC bits of this control D register.

30 SEC (D3) Setting this bit to '1' will change the time to the closest minute. This bit will return to '0' when the clock/calendar can be accessed again. No reading from or writing to the time and day registers maybe done during the 125 microseconds necessary to make this adjustment.

MASK (D0) This bit masks the STD.P output. Writing a '1' disables the output, '0' enables it.

IRT/ST (D1) This bit changes the STD.P mode. When this bit is a '1' , normal interrupt mode is chosen. When this bit is a '0', a cyclic wave form is output determined by T0 and T1 (Figure 28).

Cyclic Wave Form Period			
T0	**T1**	**Period**	**Duty Cycle of '0' level ('1' level = 7.8125 milliseconds)**
0	0	1/64 second	1/2
0	1	1 second	1/128
1	0	1 minute	1/7680
1	1	1 hour	1/460800

Figure 28: Interrupt Wave Form Timing

9.3 Control F Register

REST (D0) A '1' written to this bit will clear the clock's internal divider counter of less than 1 second. A '0' will release the counter.
STOP (D1) A '1' written to this bit will stop all carries into the counter inhibiting timing. Writing a '0' enables carries (delay of 122 microseconds maximum depending on time for next carry).

24/12 (D2) A '1' indicates 24-hour mode (PM/AM invalid) and a '0' indicates 12-hour mode (PM/AM valid).

TEST (D3) Setting this bit to a '1' clocks the seconds at 5416.3 Hz. This is for testing purposes only.

9.4 Sample BASIC-52 Program for the Clock/Calendar

The following program demonstrates reading and writing to the M6242B.

```
 10 STRING 71,9 : DIM T(15)
 20 $(0)="Sunday" : $(1)="Monday" : $(2)="Tuesday : $(3)="Wednesday"
 30 $(4)="Thursday" : $(5)="Friday" : $(6)="Saturday"
 40 XBY(0E02FH)=4
 50 GOSUB 300
 60 GOSUB 350
 70 ?
 80 ?"Hit MENU Selection #"
 90 ?"1 - Set Seconds 0-59"
100 ?"2 - Set Minutes 0-59"
110 ?"3 - Set Hours 1-24"
120 ?"4 - Set Day 1-31"
130 ?"5 - Set Month 1-12"
140 ?"6 - Set Year 00-99"
150 ?"7 - Set Day of Week 0=SUN 1=MON 2=TUE"
160 ?"8 - Read Clock & Calendar"
170 ?"9 - End"
180 G=GET
190 G=GET
200 IF G=0 THEN 190
210 G=G-30H
220 IF ((G<1).OR.(G>9)) THEN 190
230 IF G=9 THEN END
240 IF G=8 THEN 50
250 INPUT "Enter Value"V
260 IF G=7 THEN 280
```

```
270 XBY(0E020H+(G*2)-1)=INT(V/10)
280 XBY(0E020H+(G*2)-2)=V-(INT(V/10)*10)
290 GOTO 50
297 REM ****************************************
298 REM * READ ALL THE TIME AND DATE REGISTERS *
299 REM ****************************************
300 FOR X=0 TO 15
310 T(X)=(XBY(0E020H+X).AND.15)
320 IF (T(X)<>(XBY(0E020H+X).AND.15)) THEN 310
330 NEXT X
340 RETURN
347 REM ***********************************
348 REM * PRINT OUT CURRENT DATE AND TIME *
349 REM ***********************************
350 ? $(T(12)),
360 ? 10*T(9)+T(8),"/",
370 ? 10*T(7)+T(6),"/",
380 ? 10*T(11)+T(10)," ",
390 ? 10*(T(5).AND.3)+T(4),":",
400 ? 10*T(3)+T(2),":",
410 ? 10*T(1)+T(0)
420 RETURN
```

This program does not check for legal entries. Enter values as prompted by the menu. The clock is set to the 24-hour mode.

NOTE: Powering the system up or down with out the clock/calendar battery backed may cause untimely writes to the M6242B.

9.5 Interrupt Modes

The STD.P output from the M6242B can be used as an interrupt source. JP11 allows the selection of either *INT0 or *INT1 for the interrupt (Figure 29). Two modes of interrupt can be selected through the control registers D-F of the M6242B. The IRT (interrupt) mode gives a one-time interrupt while ST (standard) mode creates a recurring interrupt pulse. See control register description for the particulars.

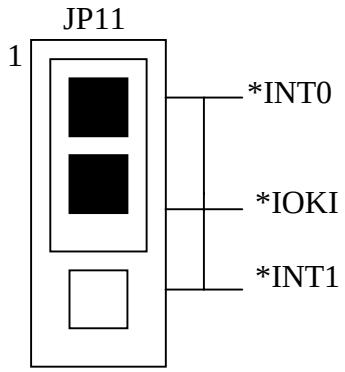
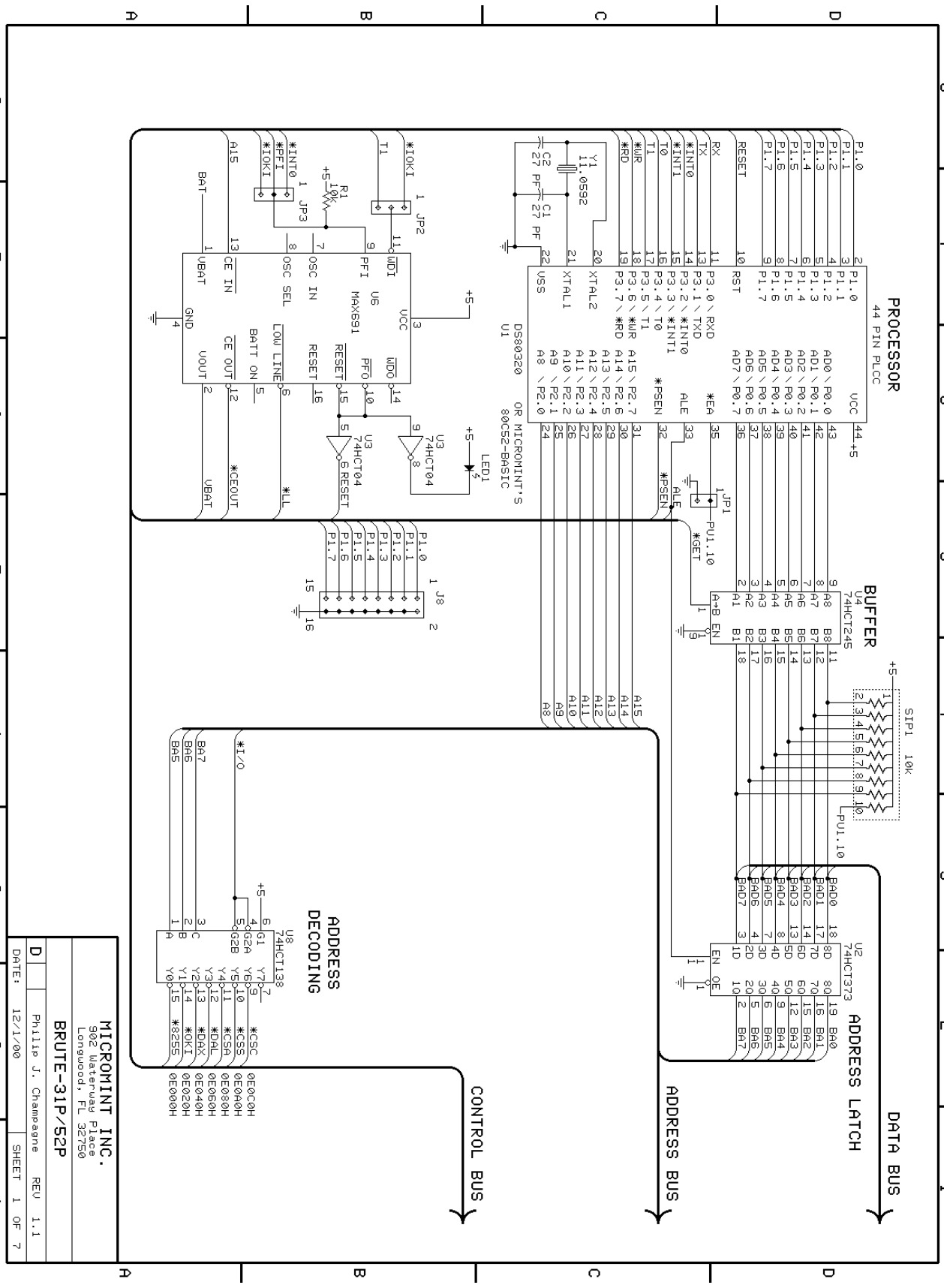
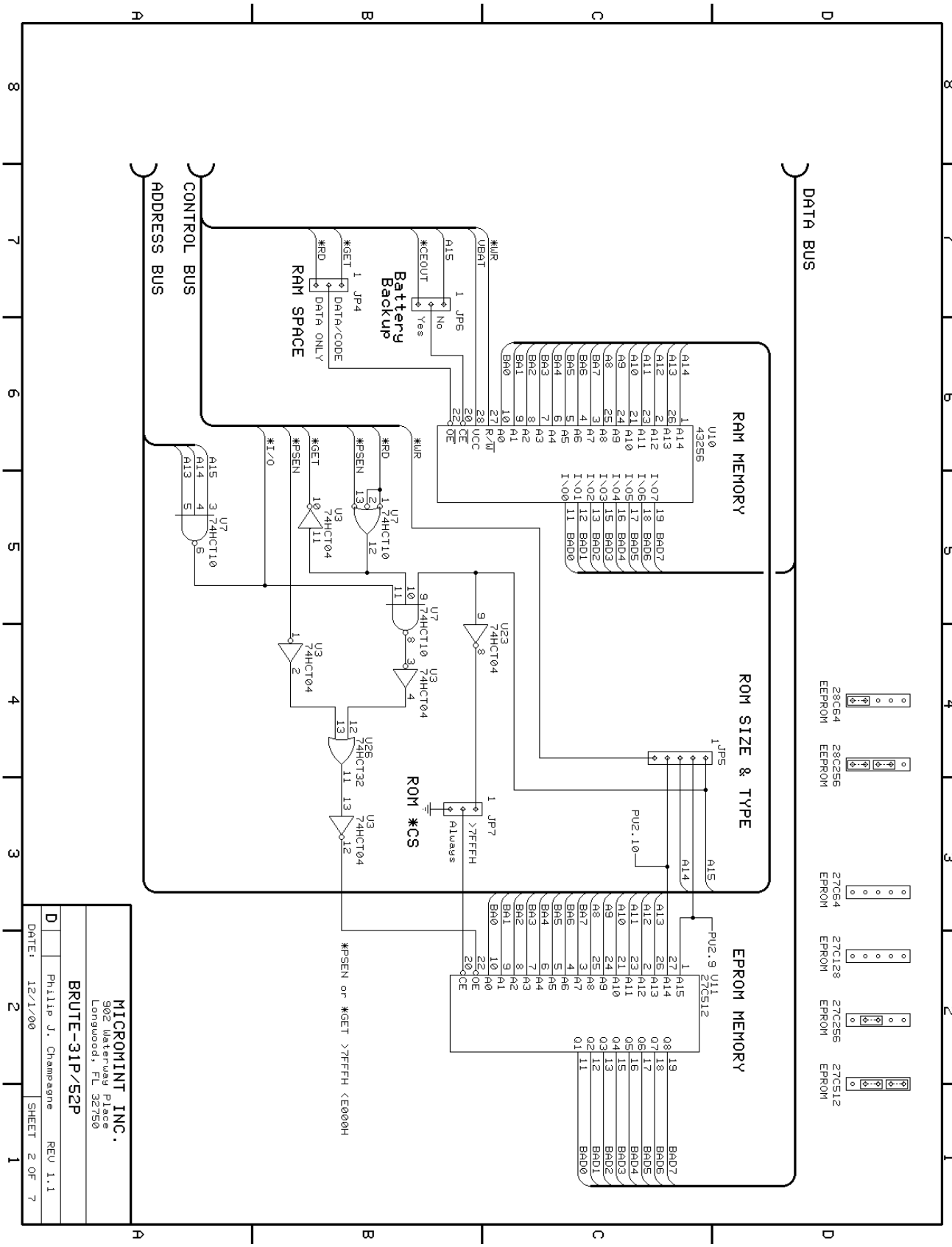
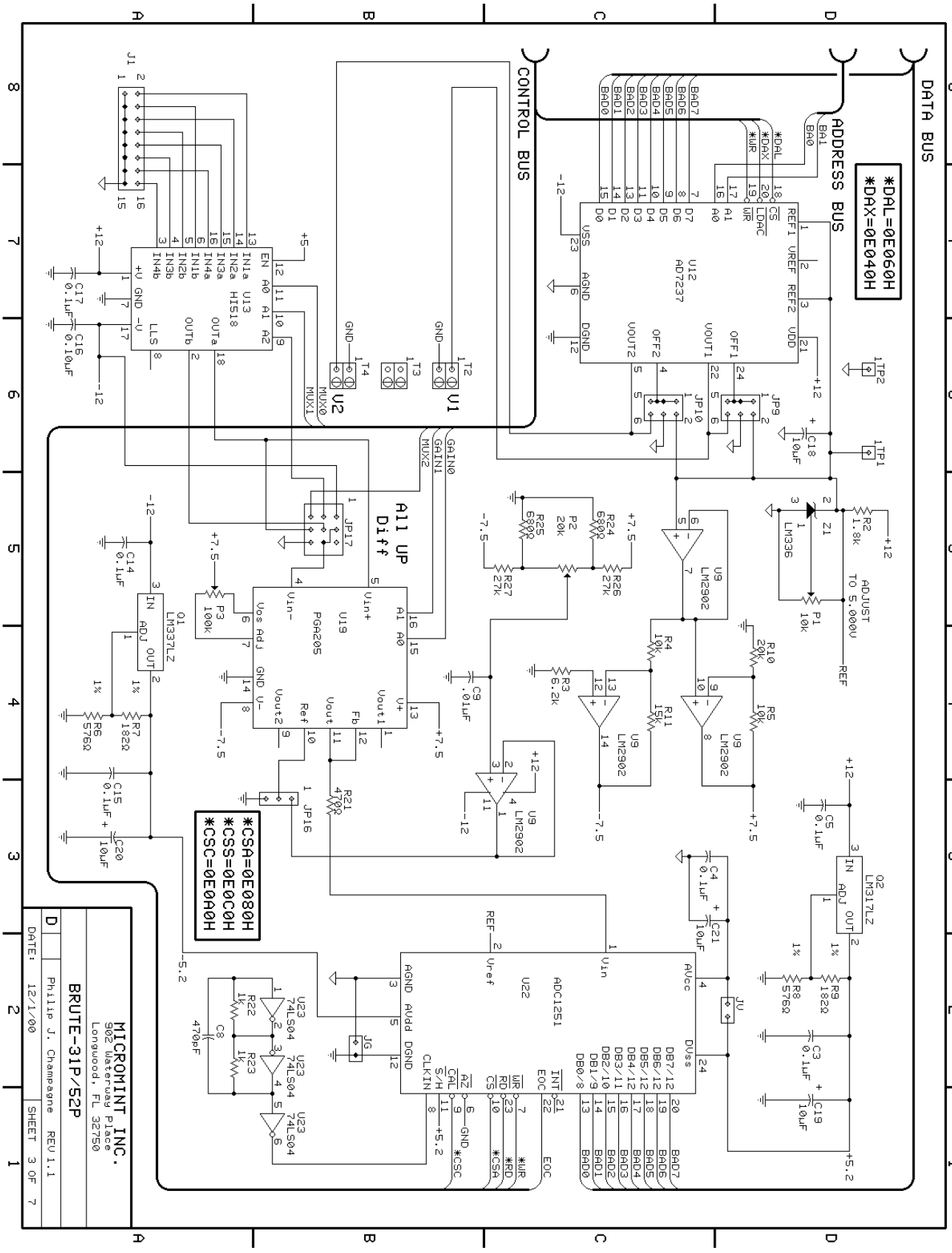
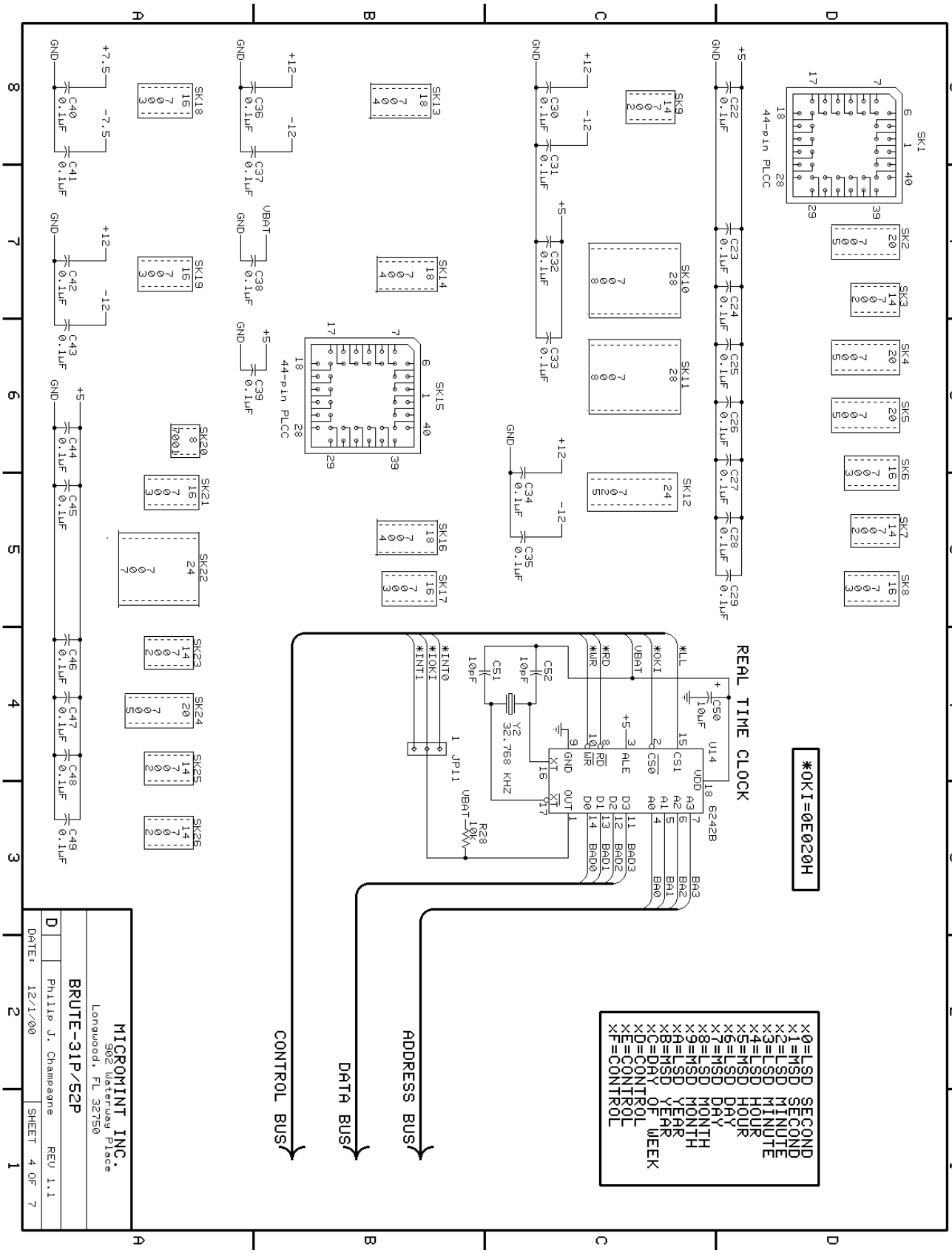


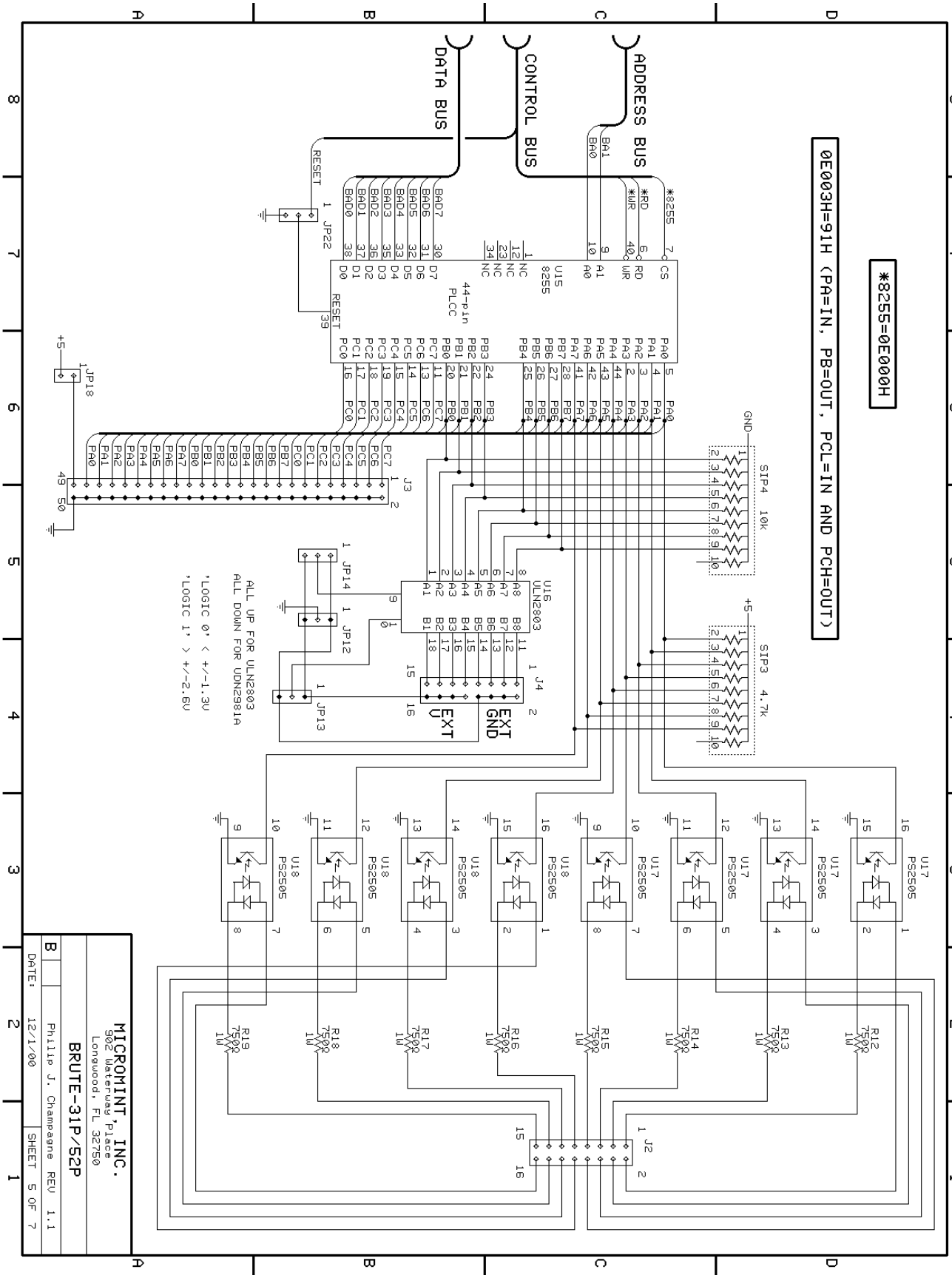
Figure 29: JP11 Clock/Calendar Interrupt Destination

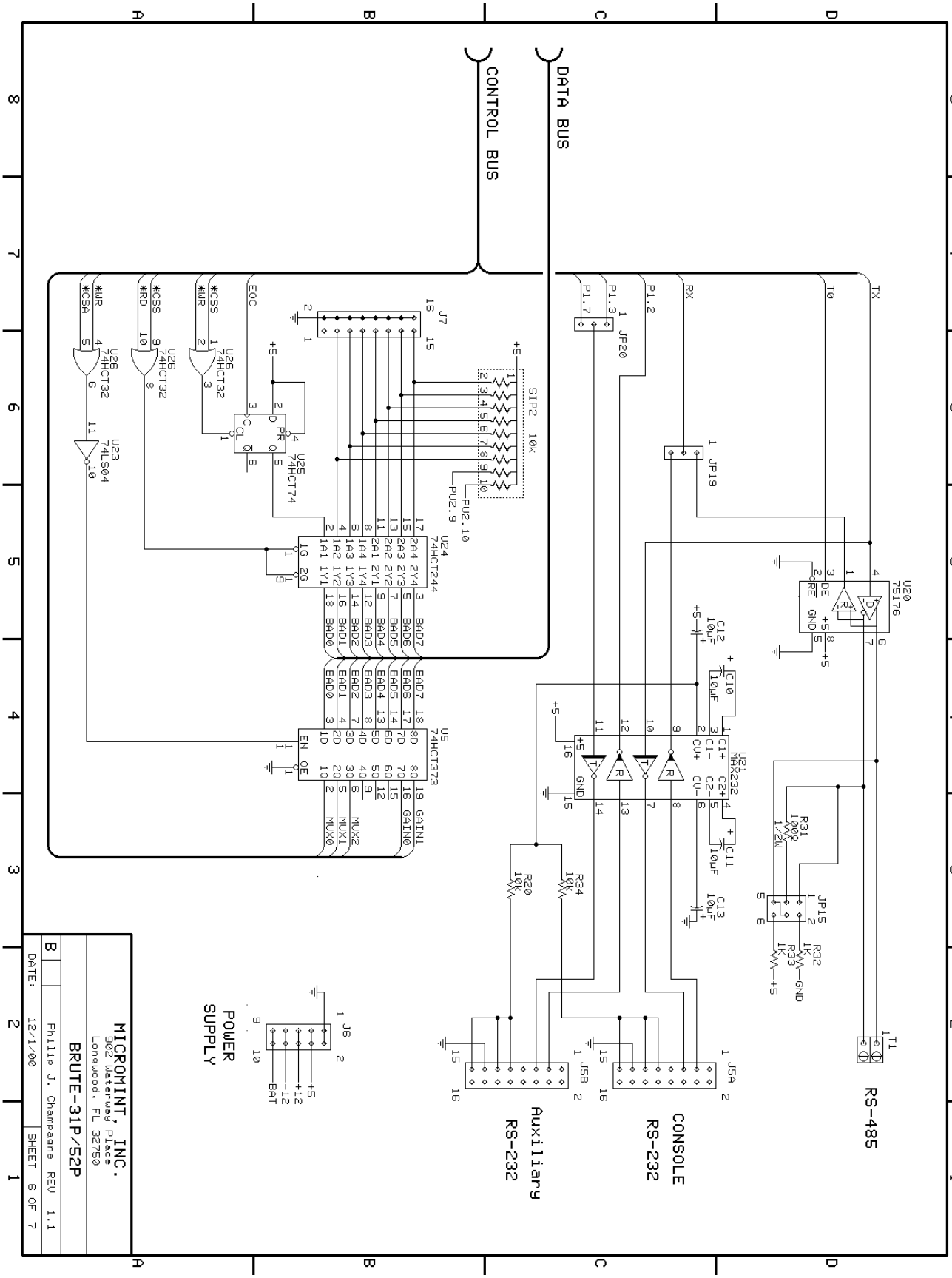

PROCESSOR
44 PIN PLCC
DS80320
U1
OR MICROMINT'S
80C52-BASIC
Y1
11.0592
C1
27 PF
C2
27 PF
XTAL1
XTAL2
RESET
RST
VCC
VSS
ALE
*PSEN
*EA
*RD
*WR
RX
TX
*INT0
*INT1
T0
T1
P1.0
P1.1
P1.2
P1.3
P1.4
P1.5
P1.6
P1.7
P3.0 \ RXD
P3.1 \ TXD
P3.2 \ *INT0
P3.3 \ *INT1
P3.4 \ T0
P3.5 \ T1
P3.6 \ *WR
P3.7 \ *RD
AD0 \ P0.0
AD1 \ P0.1
AD2 \ P0.2
AD3 \ P0.3
AD4 \ P0.4
AD5 \ P0.5
AD6 \ P0.6
AD7 \ P0.7
A8 \ P2.0
A9 \ P2.1
A10 \ P2.2
A11 \ P2.3
A12 \ P2.4
A13 \ P2.5
A14 \ P2.6
A15 \ P2.7
BUFFER
U4
74HCT245
A+B
EN
ADDRESS LATCH
U2
74HCT373
EN
OE
SIP1 10k
PU1.10
JP1
*GET
ALE
*PSEN
JP2
*IOKI
WDI
T1
JP3
*INT0
*PFI
*IOKI
R1
10k
U6
MAX691
VBAT
GND
CE IN
OSC SEL
OSC IN
PFI
WDO
PFO
RESET
LOW LINE
BATT ON
CE OUT
VOUT
BAT
A15
*CEOUT
*LL
U3
74HCT04
LED1
J8
U8
74HCT138
*I/O
BA7
BA6
BA5
*CSC
*CSS
*CSA
*DAL
*DAX
*OKI
*8255
0E0C0H
0E0A0H
0E080H
0E060H
0E040H
0E020H
0E000H
DATA BUS
ADDRESS BUS
CONTROL BUS
ADDRESS
DECODING
MICROMINT INC.
902 Waterway Place
Longwood, FL 32750
BRUTE-31P/52P
Philip J. Champagne
12/1/00
REV 1.1
SHEET 1 OF 7

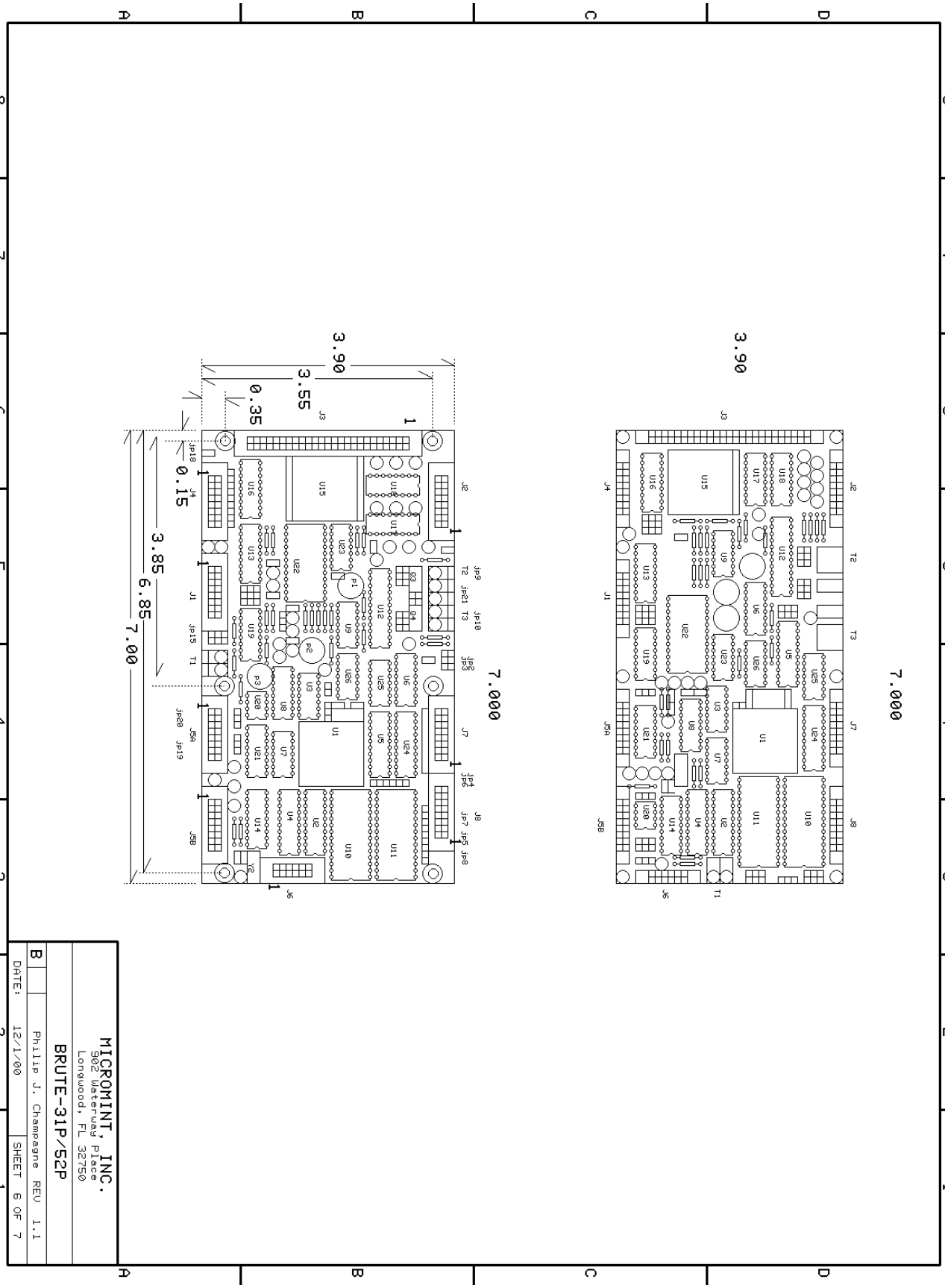

DATA BUS
CONTROL BUS
ADDRESS BUS
RAM MEMORY
ROM SIZE & TYPE
EPROM MEMORY
ROM *CS
RAM SPACE
Battery Backup
U10 43256
U11 27C512
JP5
JP4
JP6
JP7
U7 74HCT10
U3 74HCT04
U23 74HCT04
U26 74HCT32
*PSEN or *GET >7FFFH <E000H
MICROMINT INC.
902 Waterway Place
Longwood, FL 32750
BRUTE-31P/52P
Philip J. Champagne
DATE: 12/1/00
REV 1.1
SHEET 2 OF 7


DATA BUS
ADDRESS BUS
CONTROL BUS
*DAL=0E060H
*DAX=0E040H
*CSA=0E080H
*CSS=0E0C0H
*CSC=0E0A0H
All UP Diff
ADJUST TO 5.000V
MICROMINT INC.
902 Waterway Place
Longwood, FL 32750
BRUTE-31P/52P
Philip J. Champagne
DATE: 12/1/00
REV 1.1
SHEET 3 OF 7


*OKI=0E020H
REAL TIME CLOCK
X0=LSD SECOND
X1=MSD SECOND
X2=LSD MINUTE
X3=LSD MINUTE
X4=LSD HOUR
X5=MSD HOUR
X6=LSD DAY
X7=MSD DAY
X8=LSD MONTH
X9=MSD MONTH
XA=LSD YEAR
XB=MSD YEAR
XC=DAY OF WEEK
XD=CONTROL
XE=CONTROL
XF=CONTROL
CONTROL BUS
DATA BUS
ADDRESS BUS
MICROMINT INC.
502 Waterway Place
Longwood, FL 32750
BRUTE-31P/52P
Philip J. Champagne
DATE: 12/1/00
REV 1.1
SHEET 4 OF 7


0E003H=91H (PA=IN, PB=OUT, PCL=IN AND PCH=OUT)
*8255=0E000H
DATA BUS
CONTROL BUS
ADDRESS BUS
U15 8255
44-pin PLCC
SIP4 10k
SIP3 4.7k
U16 ULN2803
ALL UP FOR ULN2803
ALL DOWN FOR UDN2981A
'LOGIC 0' < +/-1.3V
'LOGIC 1' > +/-2.6V
EXT GND
EXT V
U17 PS2505
U18 PS2505
MICROMINT, INC.
580 Waterway Place
Longwood, FL 32750
BRUTE-31P/52P
Philip J. Champagne REV 1.1
DATE: 12/1/00
SHEET 5 OF 7


DATA BUS
CONTROL BUS
RS-485
CONSOLE
RS-232
Auxiliary
RS-232
POWER
SUPPLY
MICROMINT, INC.
502 Waterway Place
Longwood, FL 32750
BRUTE-31P/52P
Philip J. Champagne REV 1.1
DATE: 12/1/00
SHEET 6 OF 7


3.90
3.55
0.35
0.15
3.85
6.85
7.00
7.000
3.90
7.000
MICROMINT, INC.
902 Waterway Place
Longwood, FL 32750
BRUTE-31P/52P
Philip J. Champagne REV 1.1
DATE: 12/1/00
SHEET 6 OF 7

10.1 Parts Location List

Designation	Part#
Integrated Circuits	
U1	80C31/80C52
U2,U5	74HCT373
U3,U23	74HCT04
U4	74HCT245
U6	MAX691
U7	74HCT10
U8	74HCT138
U9	LM2902
U10	62256
U11	27C64/128/256/512 or 28C64/256
U12	AD7237
U13	HI13-05-0518-8
U14	MSM6242BRS
U15	82C55
U16	ULN2803/UDN2981A
U17,U18	PS2505
U19	PGA205
U20	75176BP
U21	MAX232
U22	ADC1251CIJ
U24	74HCT244
U25	74HCT74
U26	74HCT32
Resistors	
R1,R4,R5,R20,R28,R34	10kΩ (brn-blk-org
R2	1.8kΩ (brn-gry-red
R3	6.2kΩ (blu-red-red)
R6,R8	576Ω (green-vio-blu-blk)
R7,R9	182Ω (brn-gry-red-blk
R10	20kΩ (red-blk-org
R11	15kΩ (red-green-org
R12-R19	750Ω 1watt(vio-grn-brn)
R21	470Ω (yel-vio-brn)
R22,R23,R32,R33	1kΩ (brn-blk-red
R24,R25	680 (blu-gry-brn)
R26,R27	27kΩ (red-vio-org)
R31	100Ω 1/2watt(brn-blk-brn)
P1	10kΩ Multi-turn POT
P2	100kΩ Multi-turn POT
P3	50kΩ Multi-turn POT

Designation	Part#
SIP1,SIP2,SIP4	4.7kΩ 9 Elements
SIP3	10kΩ 9Elements
Capacitors	
C1,C2	27pf Monolithic
C3-C5,C8,C14-C17,C22-C49	0.1µF 50V Monolithic
C8	470pF Ceramic
C9	0.01µF Monolithic
C10-C13,C18-C21,C50	10µF 16V Tantalum
C51,C51	10pF Monolithic
Semiconductors	
LED1	RED Light Emitting Diode
Q1	LM337LZ
Q2	LM317LZ
Z1	LM376 Z-5
Miscellaneous	
Y1	11.0592 MHz Crystal
Y2	32.768 kHz Crystal